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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/700,033	11/03/2003	Greory William Smaus	5500-91600	3398

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EXAMINER	
CODY, DILLON J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 03/14/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/700,033	SMAUS ET AL.	
	Examiner	Art Unit	
	Dillon Cody	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *03 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-23 are pending.

Papers Filed

2. Examiner acknowledges receipt of claims, disclosure, drawings, and declaration, all filed 3 November 2003.

Title

3. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Specification

4. The disclosure is objected to because of the following informalities:

Page 3, line 9: "instruction cache" should read "the instruction cache"

Appropriate correction is required.

5. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

6. Claims 2-3, 6, 9-10, and 19-23 are objected to because of the following informalities:

Claims, 2, 3, 6, 9, 10, 19, 20: "instruction cache" should be preceded by "the"

Claims 21, 22: "microprocessor" should read "method", as claim 15 is directed to a method.

Claim 23: "instruction cache" should be preceded by "an"

Appropriate correction is required.

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

8. Claims 1, 6-8, 13-18 and 23 are rejected under 35 U.S.C. 102(b) as being anticipated by Mendelson et al. (U.S. Publication No. US 2002/0095553) hereinafter referred to as Mendelson.

9. As per claim 1, Mendelson discloses a microprocessor, comprising:

an instruction cache; (Fig. 3 L2 cache 340) *The examiner asserts that the L2 cache stores instructions.*

a trace cache; (Fig. 3 FTC 320 and MTC 330)

and a prefetch unit coupled to the instruction cache and the trace cache; (Fig. 3 Cache Manager 310) *The examiner asserts that the management logic fetches instruction traces to the L2 cache in response to their being evicted from a higher-level trace cache 320 or 330.*

wherein the prefetch unit is configured to fetch a line of instructions into the instruction cache in response to a trace being evicted from the trace cache. (Paragraph 39, lines 3-6).

10. As per claim 6, Mendelson discloses the microprocessor of claim 1, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response the eviction of certain traces from trace cache if the line of instructions is already stored in instruction cache. *The examiner asserts that if an instruction trace is already stored in the L2 cache, it cannot be evicted from the trace cache, and hence, will not be refetched by the L2 cache.*

11. As per claim 7, Mendelson discloses the microprocessor of claim 1, wherein the prefetch unit is configured to inhibit the fetch of a line of instructions into the instruction cache in response the eviction of certain traces from trace cache if the evicted trace is predicted unlikely to re-execute. (Paragraph 40 lines 5-7) *The examiner asserts that Mendelson's use counter is a method of indicating if a trace is likely to be re-used.*

12. As per claim 8, Mendelson discloses a computer system, comprising:

a system memory; (Fig. 1A memory 132)

and a microprocessor coupled to the system memory, comprising:

an instruction cache; (Fig. 3 L2 cache 340) *The examiner asserts that the L2 cache stores instructions.*

a trace cache; (Fig. 3 FTC 320 and MTC 330)

and a prefetch unit coupled to the instruction cache and the trace cache; (Fig. 3 Cache Manager 310) *The examiner asserts that the management logic fetches instruction traces to the L2 cache in response to their being evicted from a higher-level trace cache 320 or 330.*

wherein the prefetch unit is configured to fetch a line of instnlctions into the instruction cache in response to a trace being evicted from the trace cache. (Paragraph 39, lines 3-6).

13. As per claim 13, Mendelson discloses a computer system containing the processor of claim 6, hence claim 13 is rejected under the same grounds as claim 6 above.

14. As per claim 14, Mendelson discloses a computer system containing the processor of claim 7, hence claim 14 is rejected under the same grounds as claim 7 above.

15. As per claim 15, Mendelson discloses a method, comprising:

evicting a trace from a trace cache; (Paragraph 39, lines 3-6).

fetching a line of instructions into an instruction cache in response to said evicting. (Paragraph 39, lines 3-6).

16. As per claim 16, Mendelson discloses the method of claim 15, further comprising checking the instruction cache for lines of instructions comprising the instructions corresponding to the evicted trace. *The examiner asserts that the processor must inherently check if a trace is already stored in the L2 cache before storing it. Storing the same trace more than once in the L2 cache is a waste of resources.*

17. As per claim 17, Mendelson discloses a method performing the function of the processor of claim 6, hence claim 17 is rejected under the same grounds as claim 6 above.

18. As per claim 18, Mendelson discloses a method performing the function of the processor of claim 7, hence claim 18 is rejected under the same grounds as claim 7 above.

19. As per claim 23, Mendelson discloses a microprocessor performing the function of the processor of claim 1, hence claim 23 is rejected under the same grounds as claim 1 above.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 2-5, 9-12, and 19-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mendelson.

22. As per claim 2, Mendelson discloses the microprocessor of claim 1, but fails to disclose wherein the prefetch unit is configured to fetch a line into instruction cache comprising instructions that correspond to operations that precede a branch in the evicted trace.

23. Official notice is taken that traces may consist of multiple branch instructions. If a trace has two ore more branch instructions in it, it is guaranteed to have at least one instruction which precedes a branch instruction.

24. Traces with multiple branch instructions are beneficial when branch prediction logic can unroll multiple loops into a single string of instructions. They provide faster processing by providing instructions which are likely to execute to the execution logic of the processor.

25. It would have been obvious to one of ordinary skill in the art at the time of invention to have included traces including multiple branch instructions in those stored in Mendelson's trace cache for the benefit of faster execution.

26. As per claim 3, Mendelson discloses the microprocessor of claim 1, but fails to disclose wherein the prefetch unit is configured to fetch a line into instruction cache comprising instructions that correspond to operations that follow a branch in the evicted trace.

27. Official notice is taken that traces may consist of multiple branch instructions. If a trace has two ore more branch instructions in it, it is guaranteed to have at least one instruction which follows a branch instruction.

28. Traces with multiple branch instructions are beneficial when branch prediction logic can unroll multiple loops into a single string of instructions. They provide faster processing by providing instructions which are likely to execute to the execution logic of the processor.

29. It would have been obvious to one of ordinary skill in the art at the time of invention to have included traces including multiple branch instructions in those stored in Mendelson's trace cache for the benefit of faster execution.

30. As per claim 4, Mendelson discloses the microprocessor of claim 1, but fails to disclose wherein the prefetch unit is configured to prefetch a plurality of lines of

instructions into the instruction cache in response to the trace being evicted from the trace cache.

31. Official notice is taken that traces commonly consist of multiple lines when stored in a cache.

32. Multiple-line traces encompass multiple instructions likely to execute in sequence. Instructions strung together across multiple lines provide more sequential instructions that a single line can provide. This provides the execution logic with a more steady stream of instructions, allowing faster processing.

33. It would have been obvious to one of ordinary skill in the art at the time of invention to have included multiple-line trace cache entries in Mendelson's invention for the benefit of faster processing.

34. When a multiple-line trace is evicted from the trace cache, it is fetched by the L2 cache, as described in paragraph 39.

35. As per claim 5, Mendelson discloses the microprocessor of claim 4, wherein the prefetch unit is configured to fetch a number of lines that is proportional to the number of branch operations comprised in the evicted trace. *The examiner asserts that no matter what number of branch operations are included in an evicted trace, the number of lines fetched by the L2 cache is in some proportion to that number.*

36. As per claim 9, Mendelson discloses a computer system containing the processor of claim 2, hence claim 9 is rejected under the same grounds as claim 2 above.

37. As per claim 10, Mendelson discloses a computer system containing the processor of claim 3, hence claim 10 is rejected under the same grounds as claim 3 above.

38. As per claim 11, Mendelson discloses a computer system containing the processor of claim 4, hence claim 11 is rejected under the same grounds as claim 4 above.

39. As per claim 12, Mendelson discloses a computer system containing the processor of claim 5, hence claim 12 is rejected under the same grounds as claim 5 above.

40. As per claim 19, Mendelson discloses a method performing the function of the processor of claim 2, hence claim 19 is rejected under the same grounds as claim 2 above.

41. As per claim 20, Mendelson discloses a method performing the function of the processor of claim 3, hence claim 20 is rejected under the same grounds as claim 3 above.

42. As per claim 21, Mendelson discloses a method performing the function of the processor of claim 4, hence claim 21 is rejected under the same grounds as claim 4 above.

43. As per claim 22, Mendelson discloses a method performing the function of the processor of claim 5, hence claim 22 is rejected under the same grounds as claim 5 above.

Conclusion

44. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Peled et al. (U.S. Patent No. 6,216,206) discloses a dedicated trace victim cache to store evicted traces for future reuse.

45. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the

objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dillon Cody whose telephone number is 571-272-8401. The examiner can normally be reached on Mon - Fri, 8 AM - 5 PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on 571-272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJC

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